Analyzing the Real Jitter Performance of an SSC Clock

Martin F. Stumpf

Market Segment Management

Rohde & Schwarz

ROHDE&SCHWARZ

Disclaimer

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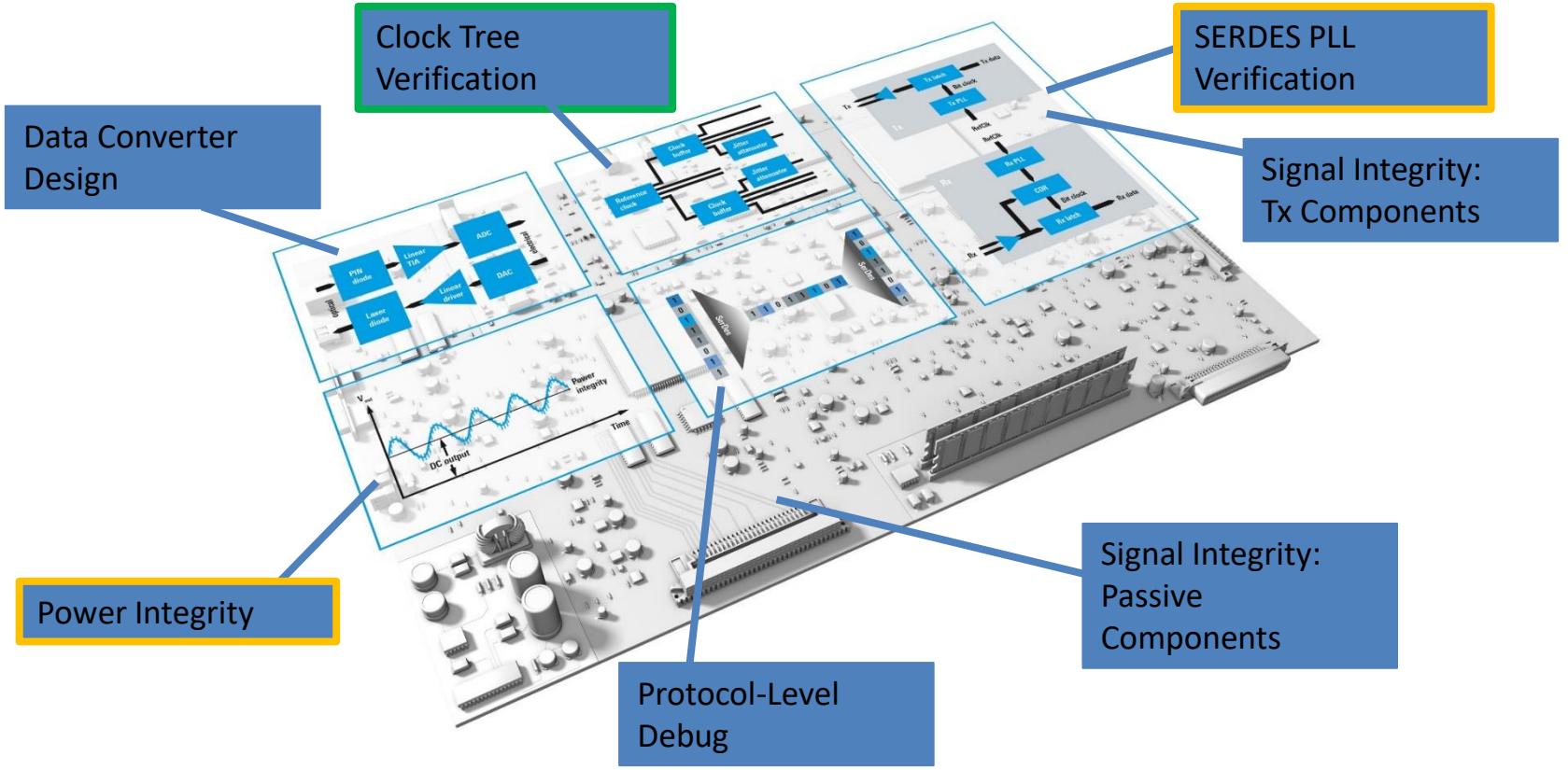
High-Speed Digital Design

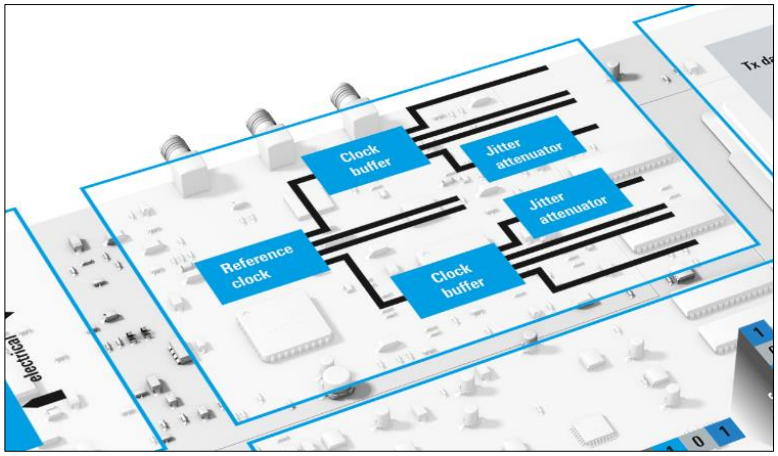
Main Building Blocks and Challenges



Clock Tree

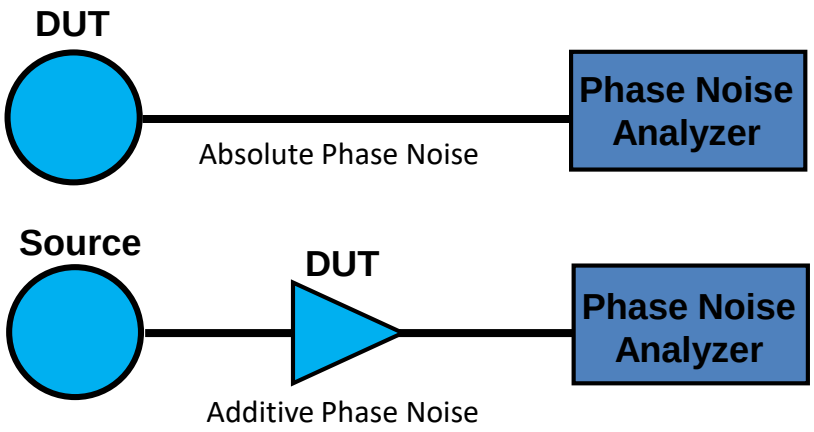
Building Blocks

- Reference clocks
- Clock buffers
- Jitter attenuators



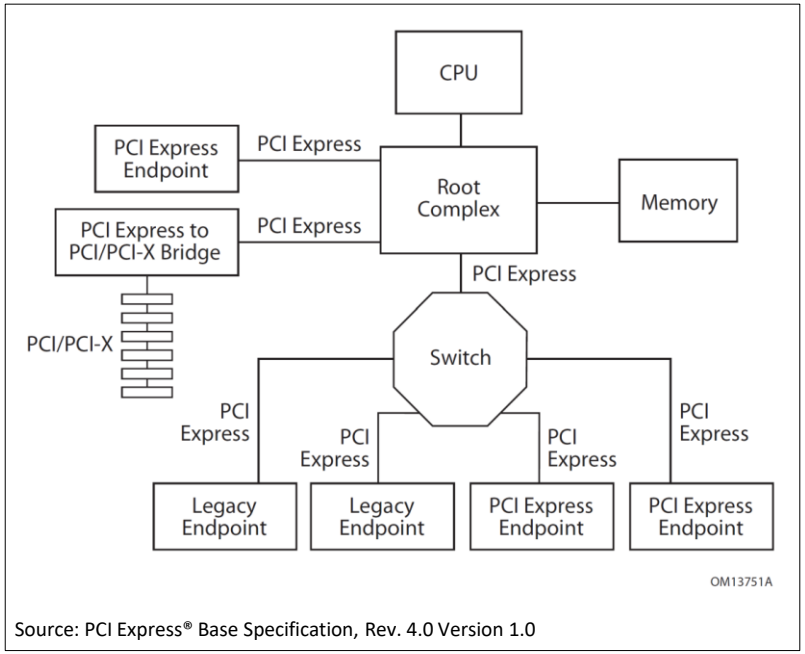
Typical Parameters

- Phase noise / jitter
- Jitter attenuation (JTF)
- Power supply noise rejection (PSNR)



PCIe® RefClk Architecture

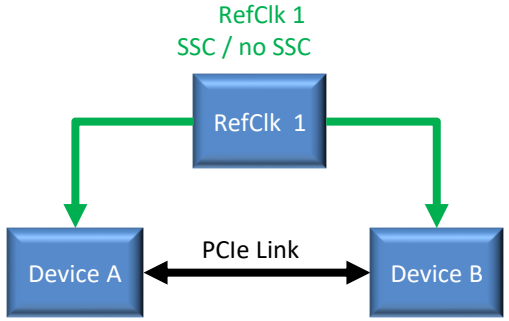
PCIe Architecture



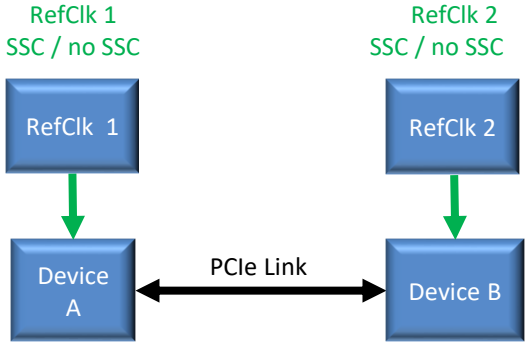
Source: PCI Express® Base Specification, Rev. 4.0 Version 1.0

RefClock Architectures

- **Common Clock (CC)**

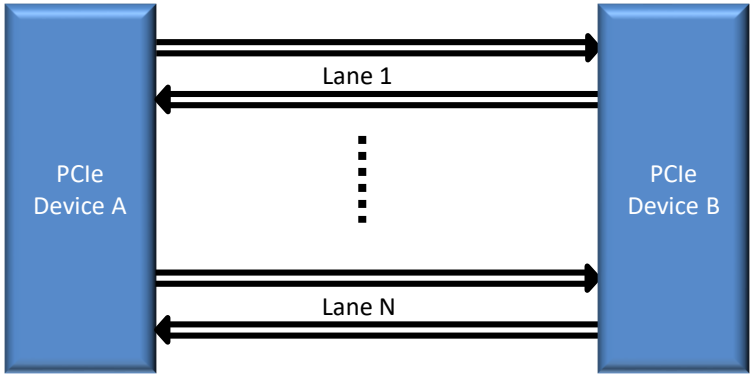


- **Separate Reference No Spread**
  Separate Reference Independent Spread



PCIe Link and RefClk Jitter

PCIe Link



PCIe Link: x1, x2, x4, x8, x12, x16, x32 lanes

PCIe link is made up of one or more lanes, each consisting of:

- 1 x differential Tx pair
- 1 x differential Rx pair

RefClk Jitter Limits

PCIe Link Speed	Refclk Jitter
2.5 GT/s	86 ps (pp)
5.0 GT/s	3.1 ps (RMS)
8.0 GT/s	1.0 ps (RMS)
16.0 GT/s	0.5 ps (RMS)
32.0 GT/s (spec. in progress)	!! tighter !!

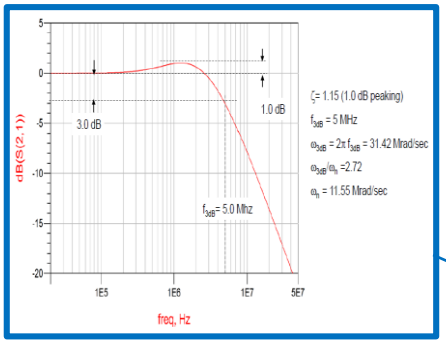
Note:

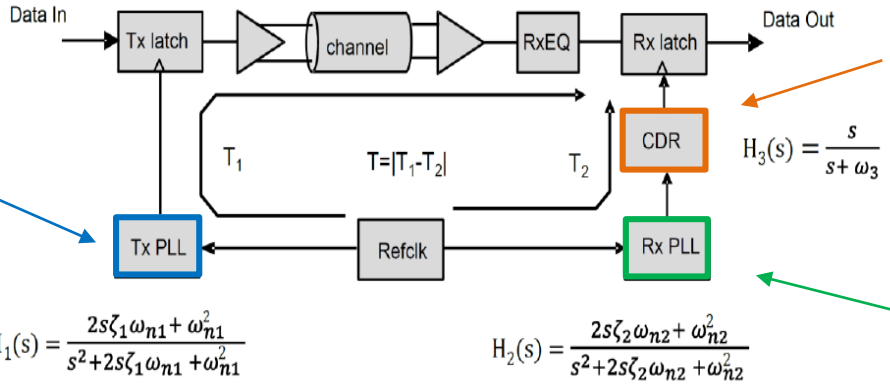
- GT/s = Gtransfers / sec

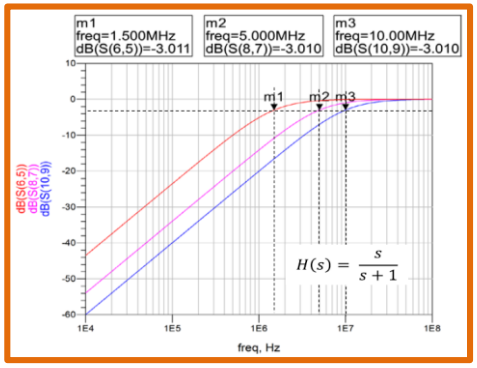
RefClk: System-Level Effects

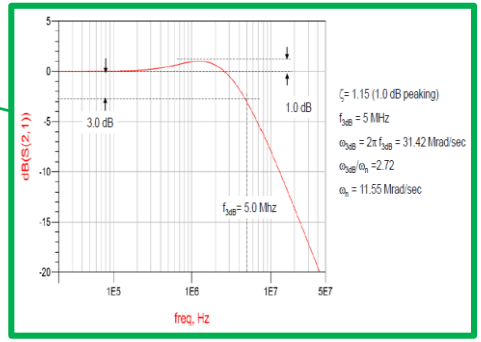
Modeling the effects at the Rx Latch:

- System Transfer Function H(s)
- Block Transfer Functions $H_1(s)$, $H_2(s)$, $H_3(s)$:









Source:
PCI Express Base Specification, Rev. 4.0 Version 1.0 (CC)

Transfer Function: $[H_1(s)e^{-sT} - H_2(s)]H_3(s)$

Jitter at Rx latch:

$X(s)[H_1(s)e^{-sT} - H_2(s)]H_3(s)$

$X(s)[H_2(s)e^{-sT} - H_1(s)]H_3(s)$

Compute both and use the larger of the two

RefClk: System-Level Effects

Modelling

- System Effect of Refclk jitter at Rx latch is modeled by the System Transfer Function H(s), consisting of:
  - Tx PLL model: $H_1(s)$
  - Rx PLL model: $H_2(s)$
  - Rx CDR model: $H_3(s)$
- For PCIe 4.0: 64 jitter results

Table 8-19: Common Refclk PLL and CDR Characteristics for 2.5 GT/s

PLL #1, PLL #2	0.01 dB peaking	3.0 dB peaking
BW_{PLL}(min) = 1.5 MHz	ω_{n1}= .336 Mrad/s, ζ_1 = 14	ω_{n1}= 5.09 Mrad/s, ζ_1 = 0.54
BW_{PLL}(max) = 22 MHz	ω_{n1}= 4.93 Mrad/s, ζ_1 = 14	ω_{n1}= 74.68 Mrad/s, ζ_1 = 0.54

BW_{CDR}(min) = 1.5 MHz, 1st order — CDR

16 combinations

2.5 GT/s

Table 8-20: Common Refclk PLL and CDR Characteristics for 5.0 GT/s

PLL #1	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 5.0 MHz	ω_{n1}= 1.12 Mrad/s, ζ_1 = 14	ω_{n1}= 11.01 Mrad/s, ζ_1 = 1.16
BW_{PLL}(max) = 16 MHz	ω_{n1}= 3.58 Mrad/s, ζ_1 = 14	ω_{n1}= 35.26 Mrad/s, ζ_1 = 1.16

PLL #2	0.01 dB peaking	3.0 dB peaking
BW_{PLL}(min) = 8.0 MHz	ω_{n2}= 1.79 Mrad/s, ζ_2 = 14	ω_{n2}= 26.86 Mrad/s, ζ_2 = 0.54
BW_{PLL}(max) = 16 MHz	ω_{n2}= 3.58 Mrad/s, ζ_2 = 14	ω_{n2}= 53.73 Mrad/s, ζ_2 = 0.54

BW_{CDR}(min) = 5 MHz, 1st order

64 combinations

5 GT/s

Table 8-21: Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1}= 0.448 Mrad/s, ζ_1 = 14	ω_{n1}= 6.02 Mrad/s, ζ_1 = 0.73
BW_{PLL}(max) = 4.0 MHz	ω_{n1}= 0.896 Mrad/s, ζ_1 = 14	ω_{n1}= 12.04 Mrad/s, ζ_1 = 0.73

PLL #2	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n2}= 0.448 Mrad/s, ζ_2 = 14	ω_{n2}= 4.62 Mrad/s, ζ_2 = 1.15
BW_{PLL}(max) = 5.0 MHz	ω_{n2}= 1.12Mrad/s, ζ_2 = 14	ω_{n2}= 11.53 Mrad/s, ζ_2 = 1.15

BW_{CDR}(min) = 10 MHz, 1st order

64 combinations

8.0, 16.0 GT/s

Source: PCI Express Base Specification, Rev. 4.0 Version 1.0

Solutions:

1) Phase Noise Analyzer
2) Phase Noise Analyzer with External Post-Processing Tool
   → export phase noise trace
   → offline post-processing

Spread Spectrum Clocking

SSC Concept:

- SSC reduces the Refclk peak power
- Slow FM to spread the power of the signal
- Jitter limits also to be met with SSC

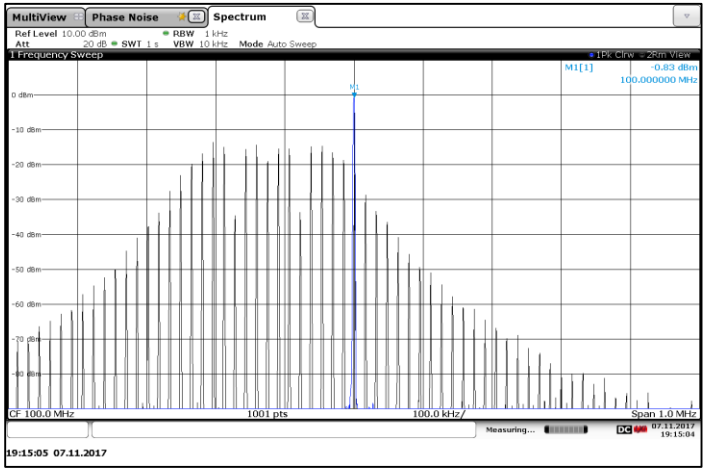
Extract from PCI Express Base Specification, Rev. 4.0 Version 1.0:

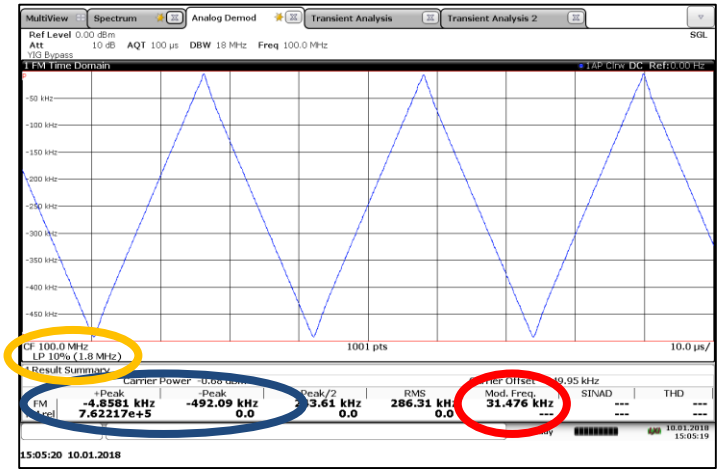
Table 8-18: Data Rate Independent Refclk Parameters

Symbol	Description	Limits	Units	Notes
F_{REFCLK}	Refclk Frequency	99.97 (min), 100.03 (max)	MHz	
F_{SSC}	SSC frequency range	30 (min), 33 (max)	kHz	
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	-0.5 (min), 0.0 (max)	%	
$T_{TRANSPORT-DELAY}$	Tx-Rx transport delay	12 (max)	ns	1, 4
$T_{SSC-MAX-FREQ-SLEW}$	Max SSC df/dt	1250	ppm/us	2, 3

Notes:

1. Parameter is relevant only for common Refclk architecture.
2. Measurement is made over 0.5µsec time interval with an 1st order LPF with an f_c of 60x the modulation frequency.
3. When testing the a device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.
4. There are form factors (for example topologies including long cables) that may exceed the transport delay limit. Extra jitter from the large transport delay must be accounted by these form factor specifications.



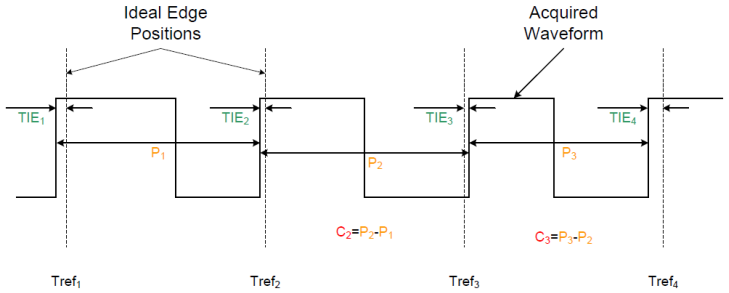


Measuring RefClk Jitter

Time Domain: Oscilloscope

- TIE Jitter Measurement:
  - Track
  - Historgam
  - Spectrum

$$j_{TIE}(n) = (t_n - t_{REF_n})$$



- Sampled Measurement (e.g. rising edge)
  → Sampling with clock frequency
  → TIE jitter spectrum shows aliasing products

- Reference: t_{REF_n}
  → Calculation based on ideal signal or selected CDR
  → TIE result includes effect of CDR Transfer Function (HP Filter)

- Relevant for Clocks: Random Jitter (RJ), Periodic Jitter (PJ) ☑

- **Limitation by Scope Jitter Noise Floor JNF**
  High Sensitivity on Clock Slew Rate

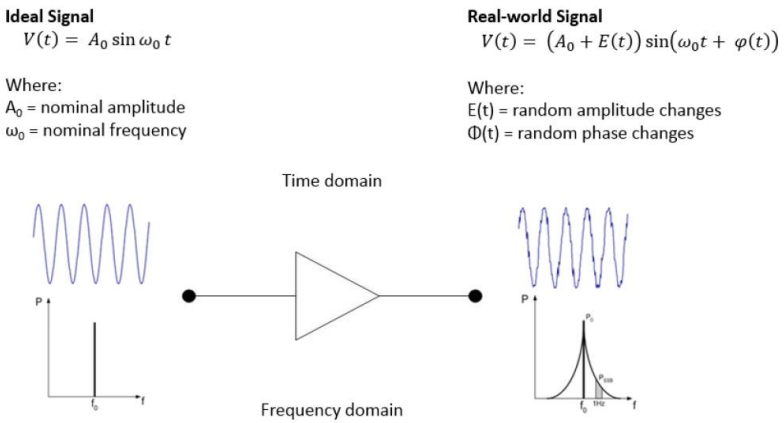
$$t_{JNF} = \sqrt{\left(\frac{V_N}{V_A \cdot r_{FS}} \cdot t_r\right)^2 + t_j^2}$$

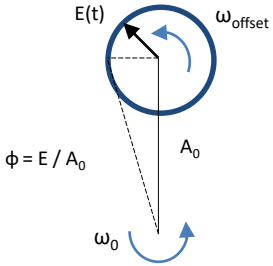
- V_N : input referred noise [V_{RMS}]
- V_A : signal amplitude [V]
- r_{FS} : full scale range
- t_r : rise time 10-90% [s]
- t_j : aperture uncertainty [s_{RMS}]

Measuring RefClk Jitter

Frequency Domain: Phase Noise Analyzer

- Phase Noise Measurement:
  - Phase Noise
  - Phase Jitter
  - → Integrate phase noise in offset-range
  - → Divide by clock-frequency ω_0

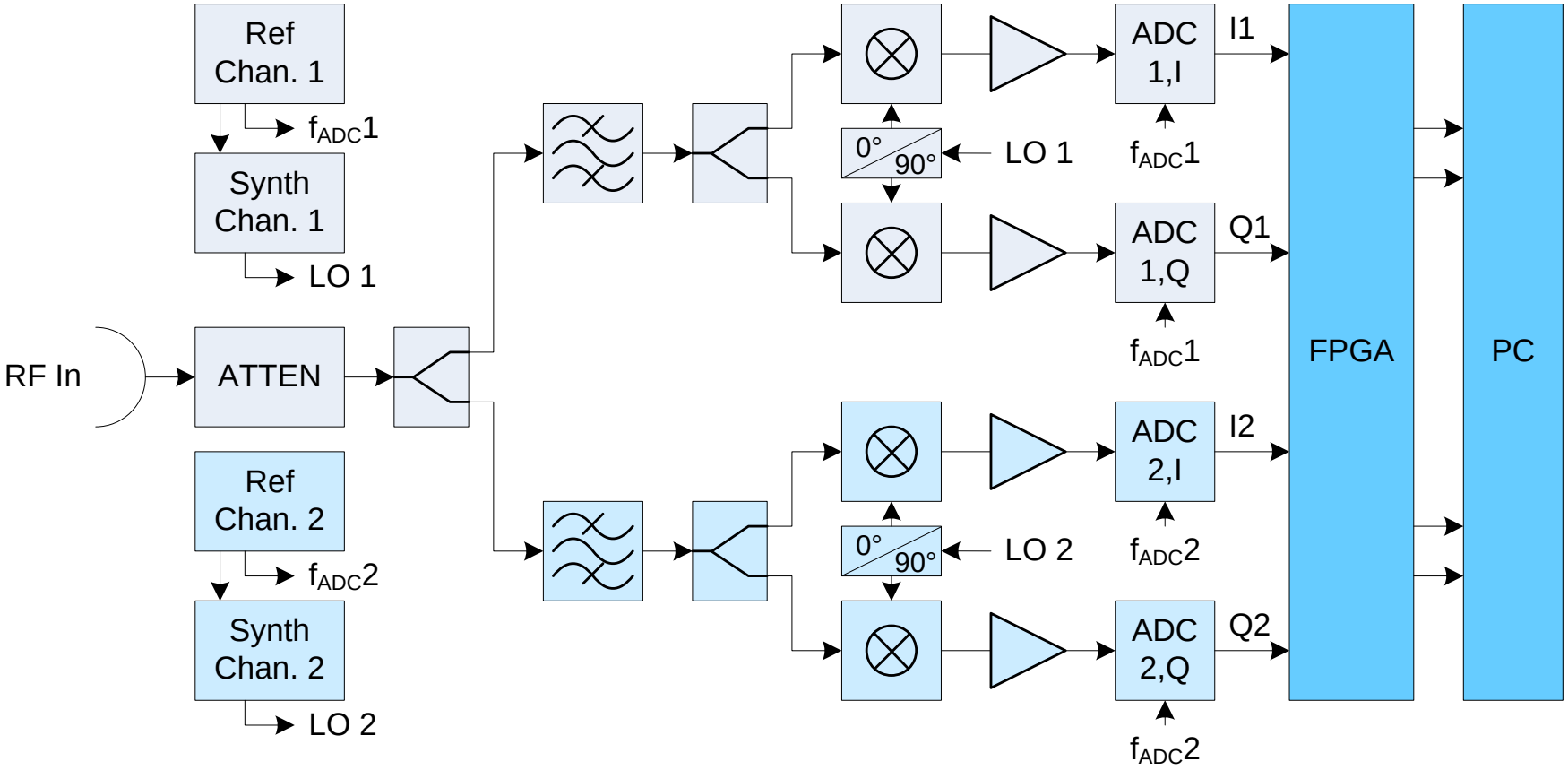




- Continuous Measurement
  - → Phase noise spectrum shows no aliasing products
- Reference: Ideal Signal
  - → Result does not include effect of CDR Transfer Function (HP Filter)
- Relevant for Clocks: Random Jitter (RJ), Periodic Jitter (PJ) ☑
- **Made for Phase Noise Testing: Outstanding Phase Noise / Jitter Performance**

Phase Noise Analyzer

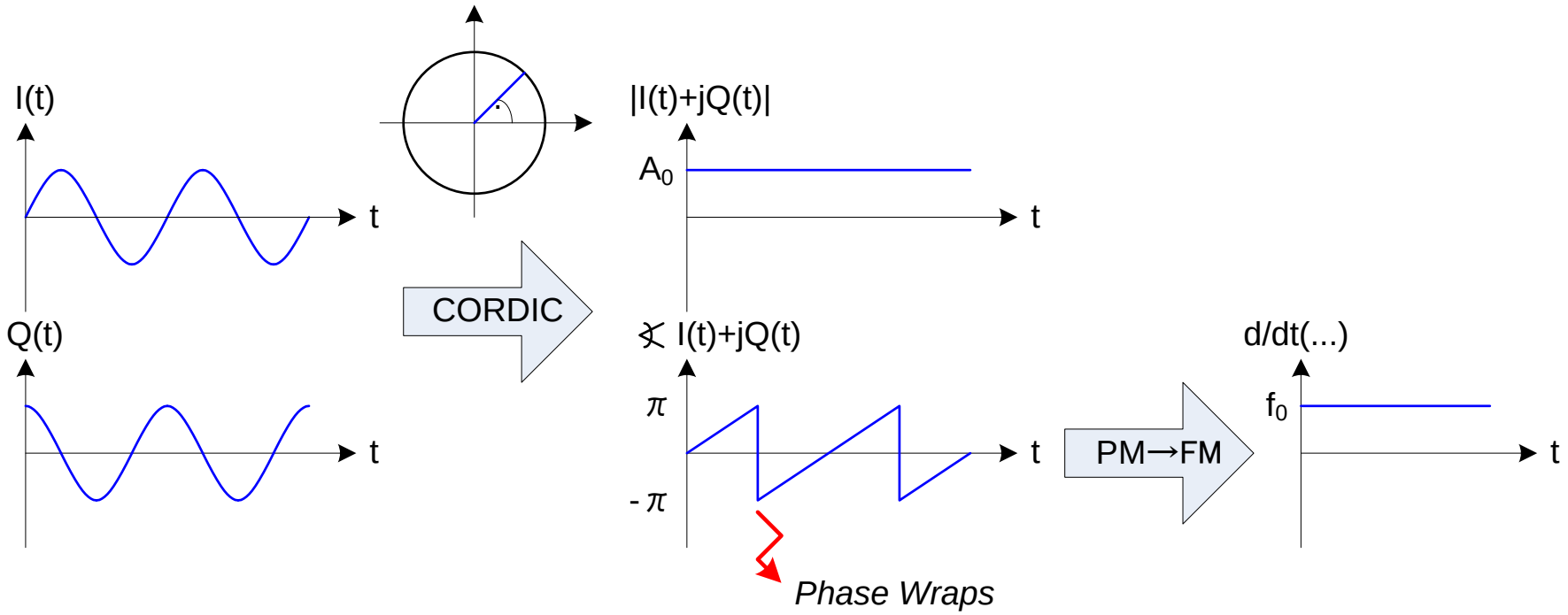
Architecture: Example R&S FSWP



Phase Noise Analyzer

Signal Processing: Example R&S FSWP

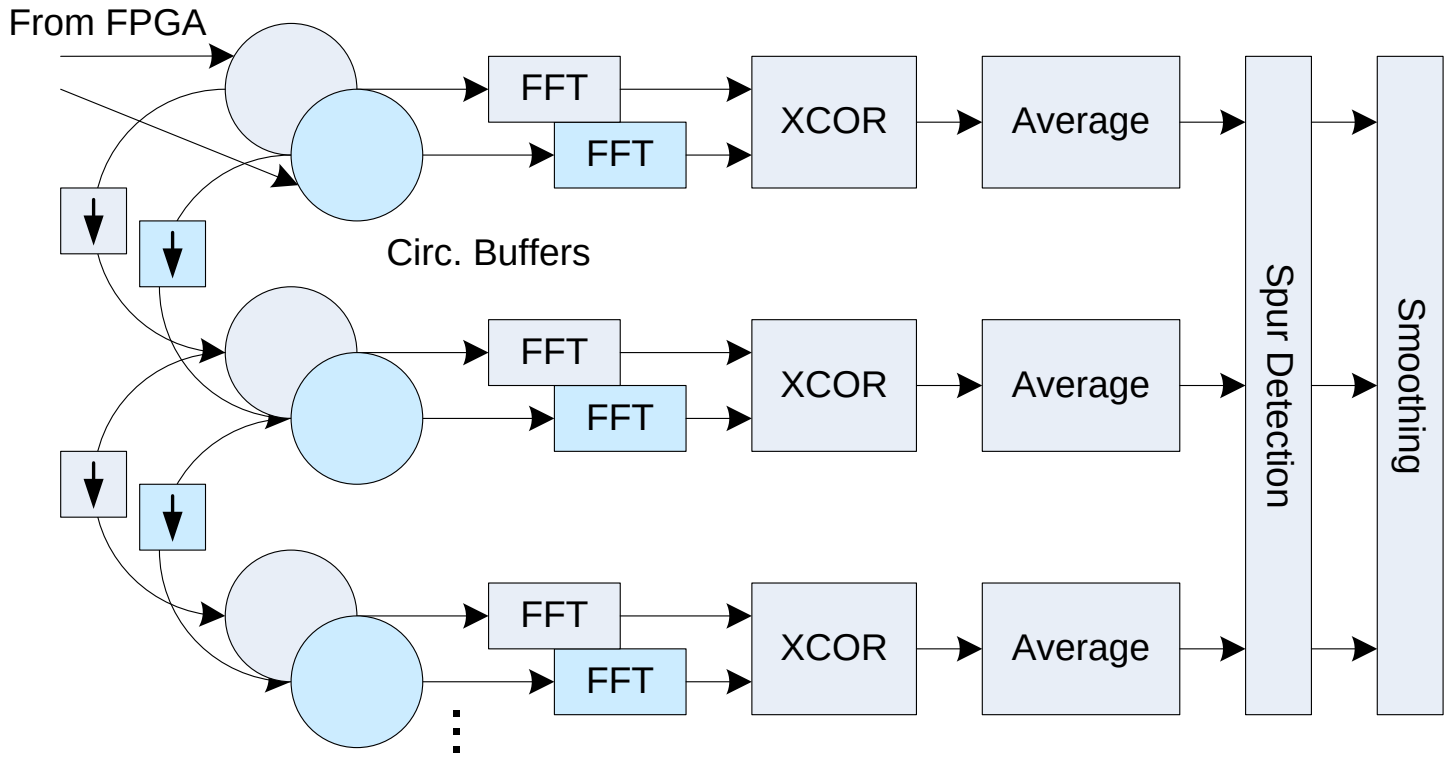
Digital Demodulation



Phase Noise Analyzer

Signal Processing: Example R&S FSWP

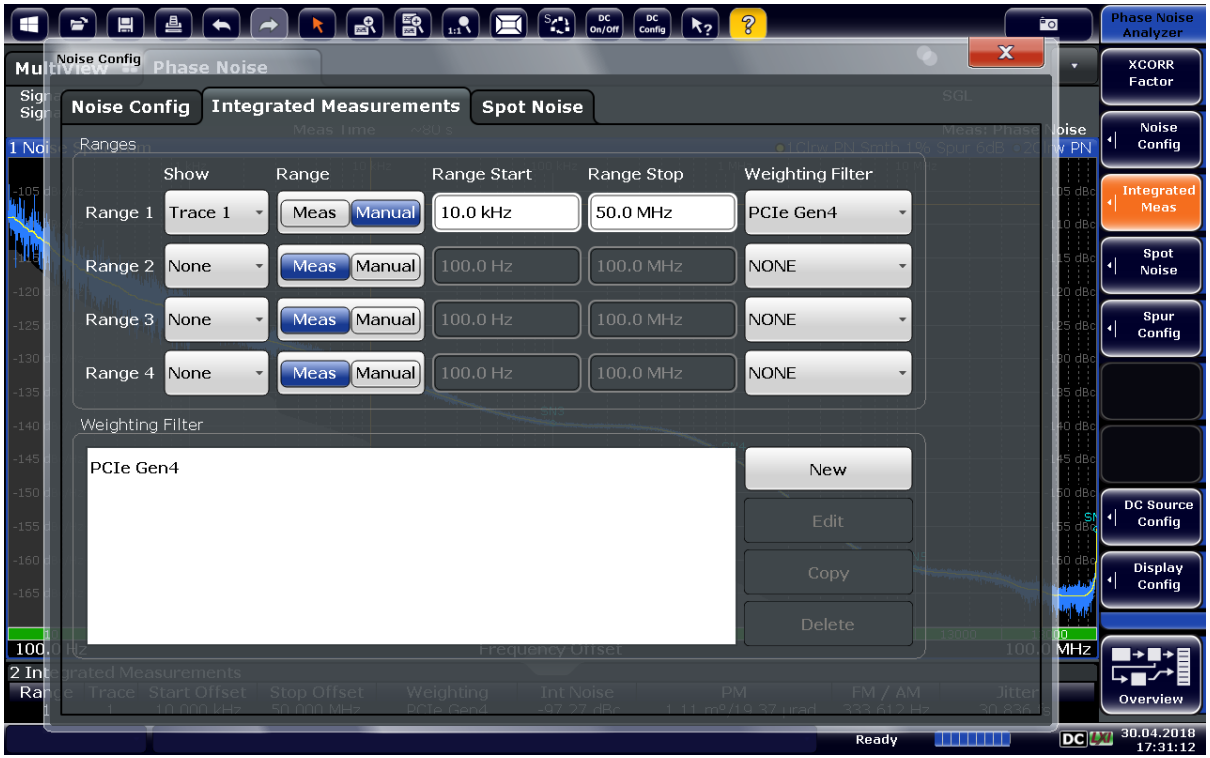
Cross-Correlation



Phase Noise Analyzer

Jitter Integration: Example R&S FSWP

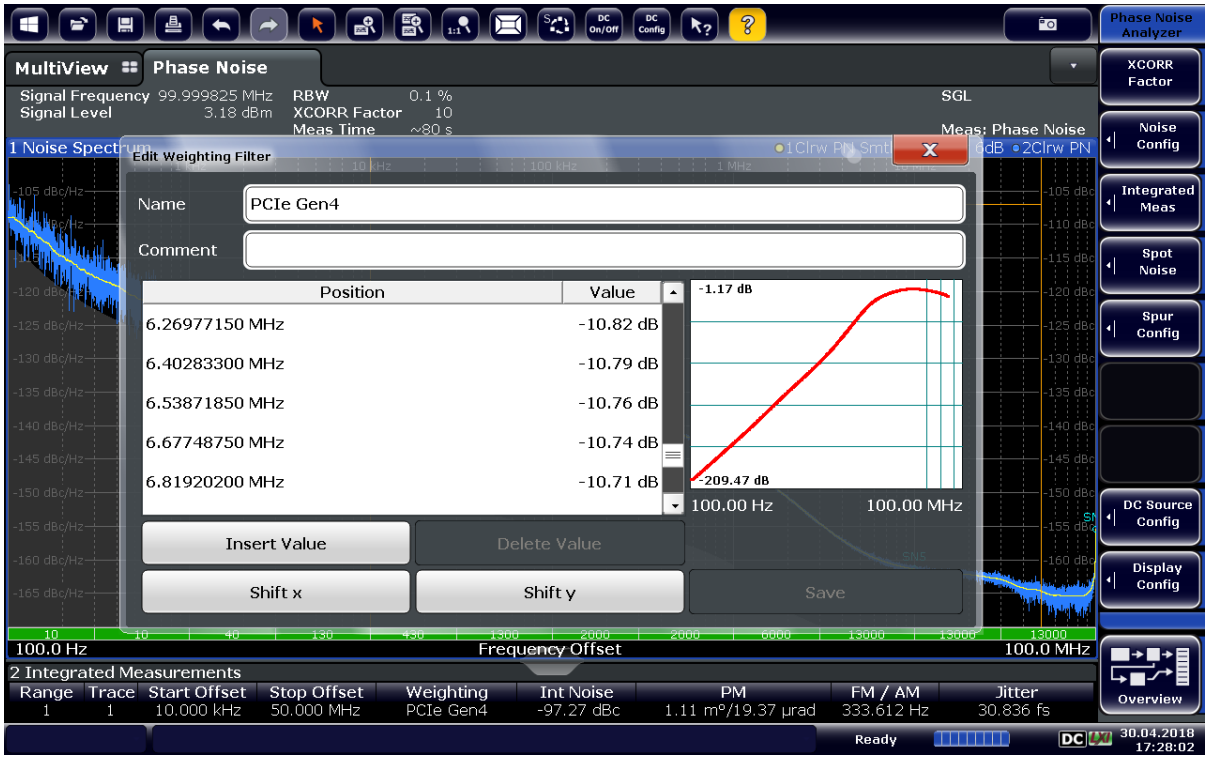
Integrated Measurement:



Phase Noise Analyzer

Jitter Weighting: Example R&S FSWP

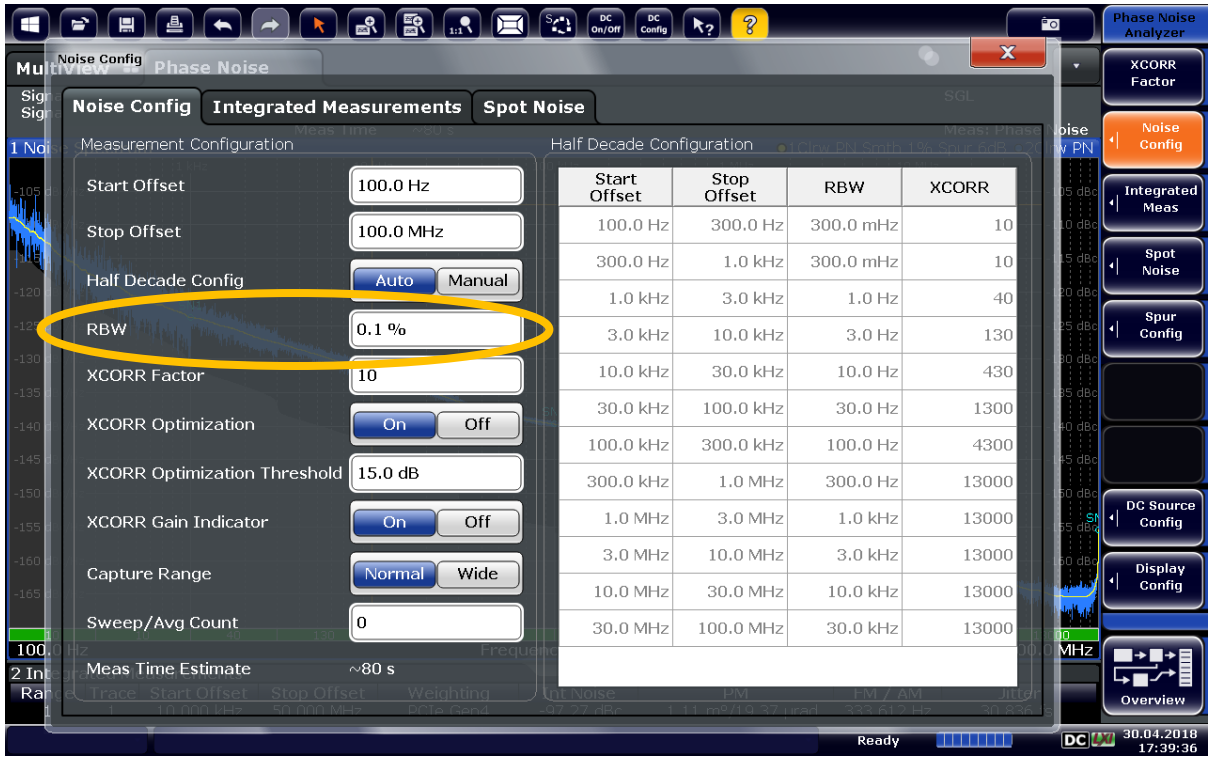
Weighting according to System Transfer Function:



Phase Noise Analyzer

Spur Detection: Example R&S FSWP

Setting for proper detection of SSC Spurs:



Low RBW:
→ Good resolution
→ SSC detection / SSC removal

PCIe RefClk Jitter: SSC OFF

Phase Noise and Jitter Results: Example R&S FSWP

Jitter Calculation:

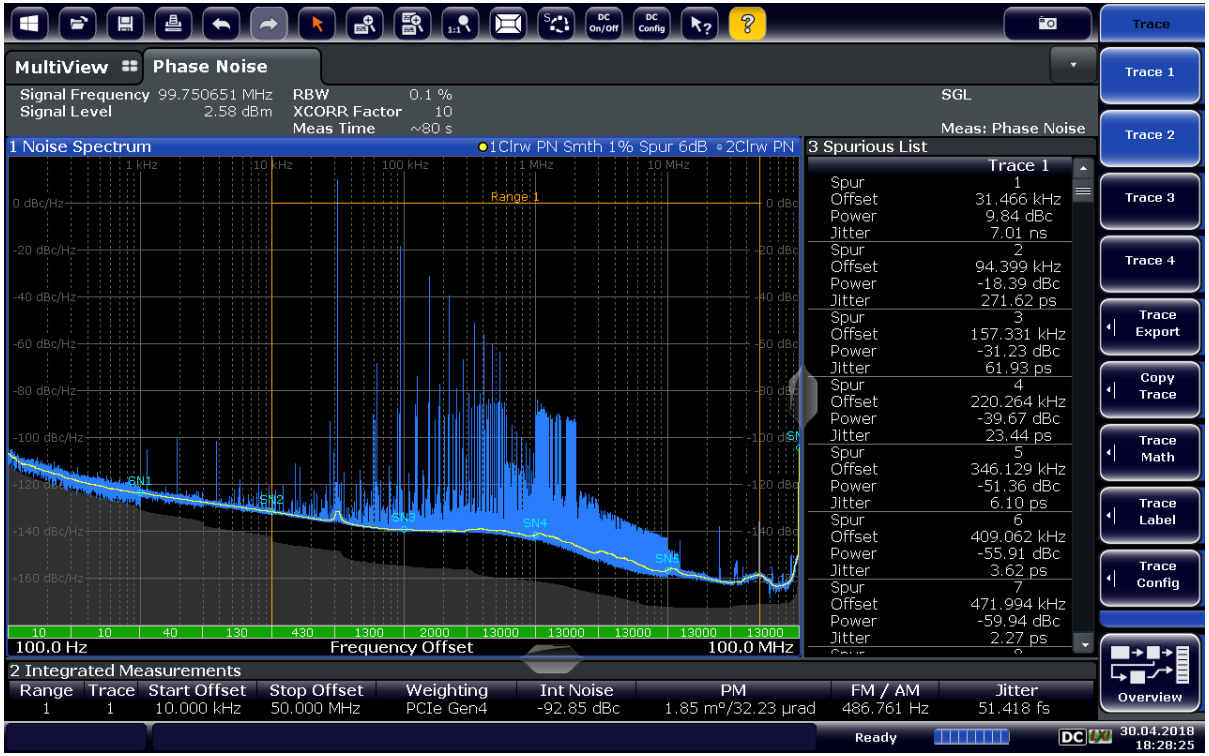
Procedure with R&S FSWP:
→ Phase noise measurement

Trace:
→ Weighting
(example: PCIe 4.0 filter)
→ Jitter integration

PCIe RefClk Jitter: SSC ON

Phase Noise and Jitter Results: Example R&S FSWP

Jitter Calculation:



Procedure with R&S FSWP:
→ Phase noise measurement

Trace:
→ Weighting
(example: PCIe Gen4 filter)
→ Jitter integration

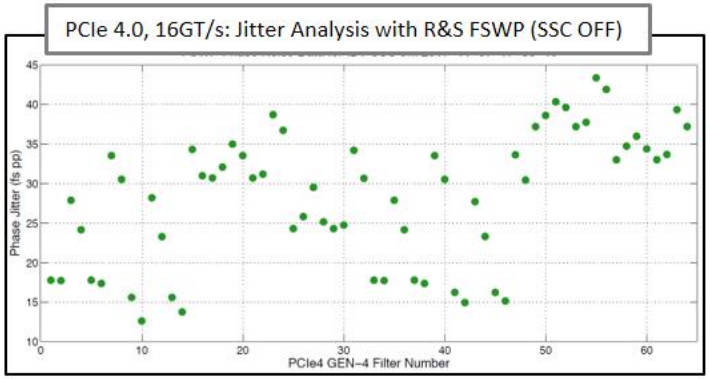
Spur List:
→ Spur processing (SSC removal)
- ≤ 2MHz: SSC removal
- > 2MHz: no removal
→ Weighting
(example: PCIe filter)
→ Jitter calculation

PCIe RefClk Jitter: SSC OFF

Post-Processing Tool: Example JitterLabs

PCIe 4.0, 16GT/s: Jitter Analysis with R&S FSWP (SSC OFF)

Spec=500 fs Units are RMS		PLL #1				PLL #2			
		Tx A	Tx B	Tx C	Tx D	Tx A	Tx B	Tx C	Tx D
PLL #1	Rx A (T1-T8)	18 fs 96 %	18 fs 96%	28 fs 94 %	24 fs 95 %	18 fs 96 %	17 fs 97 %	34 fs 93 %	31 fs 94 %
	Rx B (T9-T16)	16 fs 97 %	13 fs 97 %	28 fs 94 %	23 fs 95 %	16 fs 97 %	14 fs 97 %	34 fs 93 %	31 fs 94 %
	Rx C (T17-T24)	31 fs 94 %	32 fs 94 %	35 fs 93 %	34 fs 93 %	31 fs 94 %	31 fs 94 %	39 fs 92 %	37 fs 93 %
	Rx D (T25-T32)	24 fs 95 %	26 fs 95 %	30 fs 94 %	24 fs 95 %	24 fs 95 %	25 fs 95 %	34 fs 93 %	31 fs 94 %
PLL #2	Rx A (T33-T40)	18 fs 96 %	18 fs 96 %	28 fs 94 %	24 fs 95 %	18 fs 96 %	17 fs 97 %	34 fs 93 %	31 fs 94 %
	Rx B (T41-T48)	16 fs 97 %	15 fs 97 %	28 fs 94 %	23 fs 95 %	16 fs 97 %	15 fs 97 %	34 fs 93 %	30 fs 94 %
	Rx C (T49-T56)	37 fs 93 %	39 fs 92 %	40 fs 92 %	40 fs 92 %	37 fs 93 %	38 fs 92 %	43 fs • 91 %	42 fs 92 %
	Rx D (T57-T64)	33 fs 93 %	35 fs 93 %	36 fs 93 %	34 fs 93 %	33 fs 93 %	34 fs 93 %	39 fs 92 %	37 fs 93 %



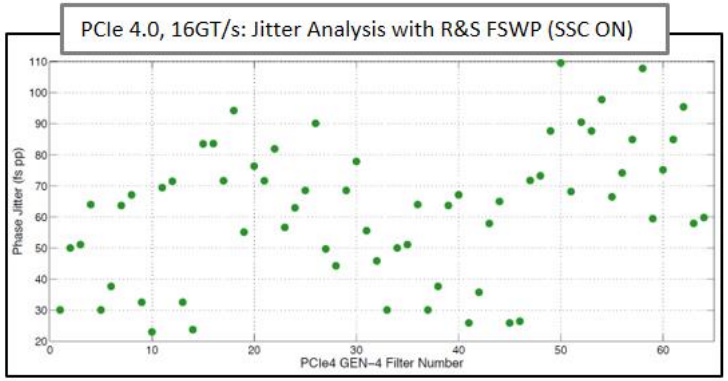
Postprocessing:
→ Export of phase noise data
→ Weighting
(64 Transfer Functions)
→ Jitter calculation
→ 64 results

PCIe RefClk Jitter: SSC ON

Post-Processing Tool: Example JitterLabs

PCIe 4.0, 16GT/s: Jitter Analysis with R&S FSWP (SSC ON)

Spec=500 fs Units are RMS		PLL #1				PLL #2			
		Tx A	Tx B	Tx C	Tx D	Tx A	Tx B	Tx C	Tx D
PLL #1	Rx A (T1-T8)	30 fs 94 %	50 fs 90 %	51 fs 90 %	64 fs 87 %	30 fs 94 %	38 fs 92 %	64 fs 87 %	67 fs 87 %
	Rx B (T9-T16)	33 fs 93 %	23 fs 95 %	69 fs 86 %	71 fs 86 %	33 fs 93 %	24 fs 95 %	83 fs 83 %	84 fs 83 %
	Rx C (T17-T24)	72 fs 86 %	94 fs 81 %	55 fs 89 %	76 fs 85 %	72 fs 86 %	82 fs 84 %	57 fs 89 %	63 fs 87 %
	Rx D (T25-T32)	69 fs 86 %	90 fs 82 %	50 fs 90 %	44 fs 91 %	69 fs 86 %	78 fs 84 %	56 fs 89 %	46 fs 91 %
PLL #2	Rx A (T33-T40)	30 fs 94 %	50 fs 90 %	51 fs 90 %	64 fs 87 %	30 fs 94 %	38 fs 92 %	64 fs 87 %	67 fs 87 %
	Rx B (T41-T48)	26 fs 95 %	36 fs 93 %	58 fs 88 %	65 fs 87 %	26 fs 95 %	26 fs 95 %	72 fs 86 %	73 fs 85 %
	Rx C (T49-T56)	88 fs 82 %	110 fs • 78 %	68 fs 86 %	91 fs 82 %	88 fs 82 %	98 fs 80 %	66 fs 87 %	74 fs 85 %
	Rx D (T57-T64)	85 fs 83 %	108 fs 78 %	59 fs 88 %	75 fs 85 %	85 fs 83 %	95 fs 81 %	58 fs 88 %	60 fs 88 %



Postprocessing:
→ Export of phase noise data
→ SSC removal
- ≤ 2MHz: SSC removal
- > 2MHz: no removal

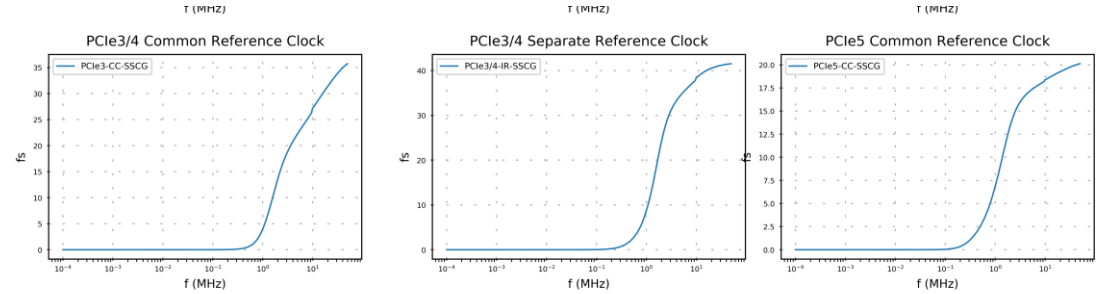
→ Weighting
(64 Transfer Functions)
→ Jitter calculation
→ 64 results

PCIe RefClk Jitter: SSC OFF

Post-Processing Tool: Example IDT (dBc2PCIe)

```
RMS Phase Jitters
------------------------------------------------------------
Total Jitter: 351.916952 (fs) | Carrier: 100.000000 (MHz)
------------------------------------------------------------
Sequence                          Value(fs)    Limit(fs)
PCIe2-CC-SSCG-LBW                     20.78      3000.00 [PASS]
PCIe2-CC-SSCG-HBW                     86.35      3100.00 [PASS]
PCIe2-IR-SSCG                        130.85      2000.00 [PASS]

PCIe3-CC-SSCG                         35.73      1000.00 [PASS]
PCIe4-CC-SSCG                         35.73       500.00 [PASS]
PCIe3/4-IR-SSCG                       41.52       700.00 [PASS]
PCIe3/4-CC4G5-SSCG                    42.97       700.00 [PASS]
PCIe5-CC-SSCG                         20.12       150.00 [PASS]
```



App Version: v1.0

Output File: RPJ$022_PN_100M_HCSL_out0_3300mV$05-01-2018-23h22m27s_page1.png

Confidential Information

Postprocessing:

→ Export of phase noise data (csv file)

→ Run dBc2PCIe program
- Automatic SSC detection
- Weighting

(64 Transfer Functions – PCIe 3.0/4.0)

→ Jitter calculation

→ 64 results

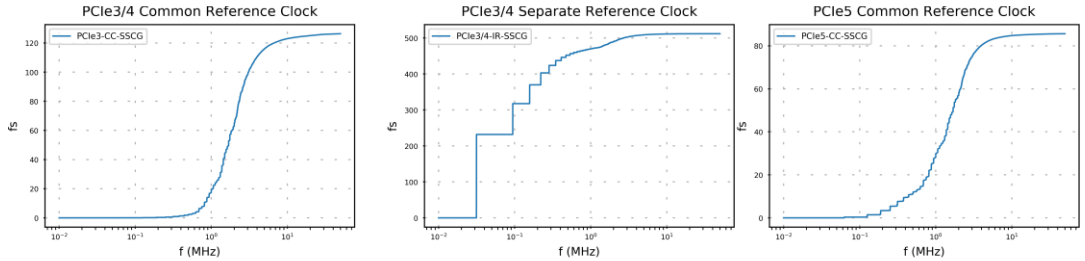
→ PNG file:
reports worst case of all applicable

PCIe RefClk Jitter: SSC ON

Post-Processing Tool: Example IDT (Bc2PCIe)

```
RMS Phase Jitters
-----------------------------------------------------------
Total Jitter: 6636702.804229 (fs) | Carrier: 100.000000 (MHz)
-----------------------------------------------------------
Sequence                        Value(fs)    Limit(fs)
PCIe2-CC-SSCG-LBW                  88.81      3000.00 [PASS]
PCIe2-CC-SSCG-HBW                 279.27      3100.00 [PASS]
PCIe2-IR-SSCG                    1360.88      2000.00 [PASS]

PCIe3-CC-SSCG                     126.35      1000.00 [PASS]
PCIe4-CC-SSCG                     126.35       500.00 [PASS]
PCIe3/4-IR-SSCG                   511.89       700.00 [PASS]
PCIe3/4-CC4G5-SSCG                143.66       700.00 [PASS]
PCIe5-CC-SSCG                      85.62       150.00 [PASS]
```



App Version: v1.0

Output File: RPJ$Trace2_data$05-01-2018-21h48m18s_page1.png

Postprocessing:

→ Export of phase noise data (csv file)

→ Run dBc2PCIe program

- Automatic SSC detection
- Weighting

(64 Transfer Functions – PCIe 3.0/4.0)

→ Jitter calculation

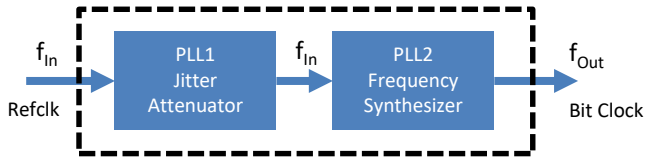
→ 64 results

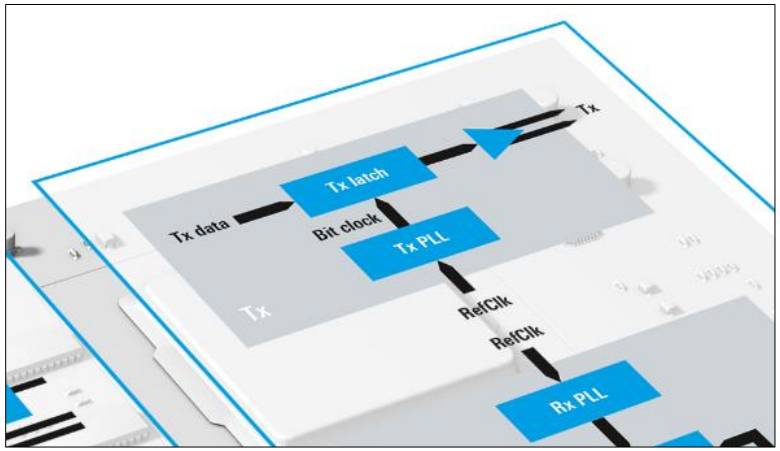
→ PNG file:
reports worst case of all applicable

Related Aspects: SerDes PLL

Building Blocks

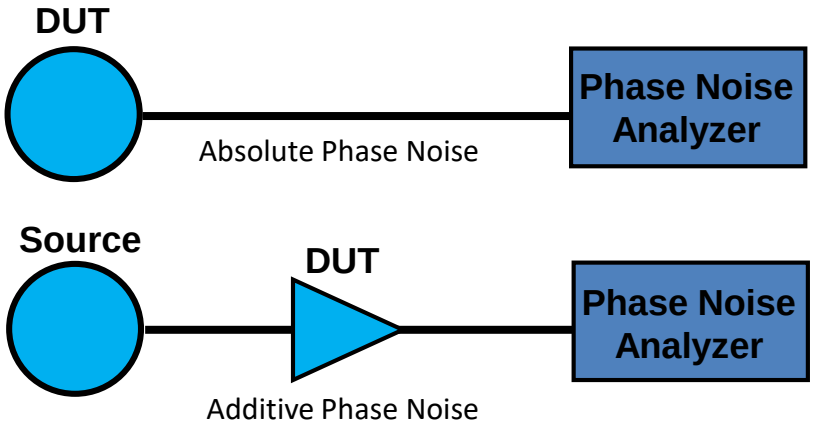
- Often two-stage architecture





Typical Parameters

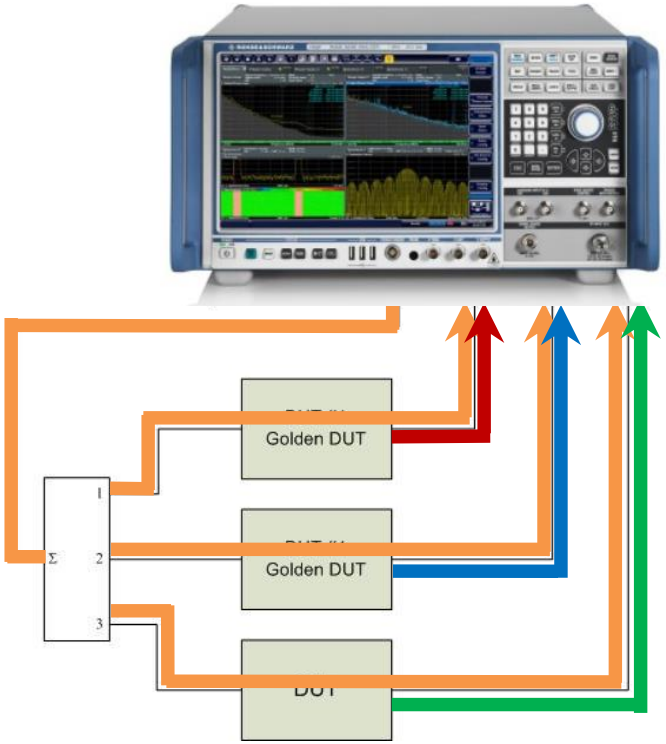
- Phase noise / jitter
- Jitter attenuation (JTF)
- System margin testing
- Power supply noise rejection (PSNR)

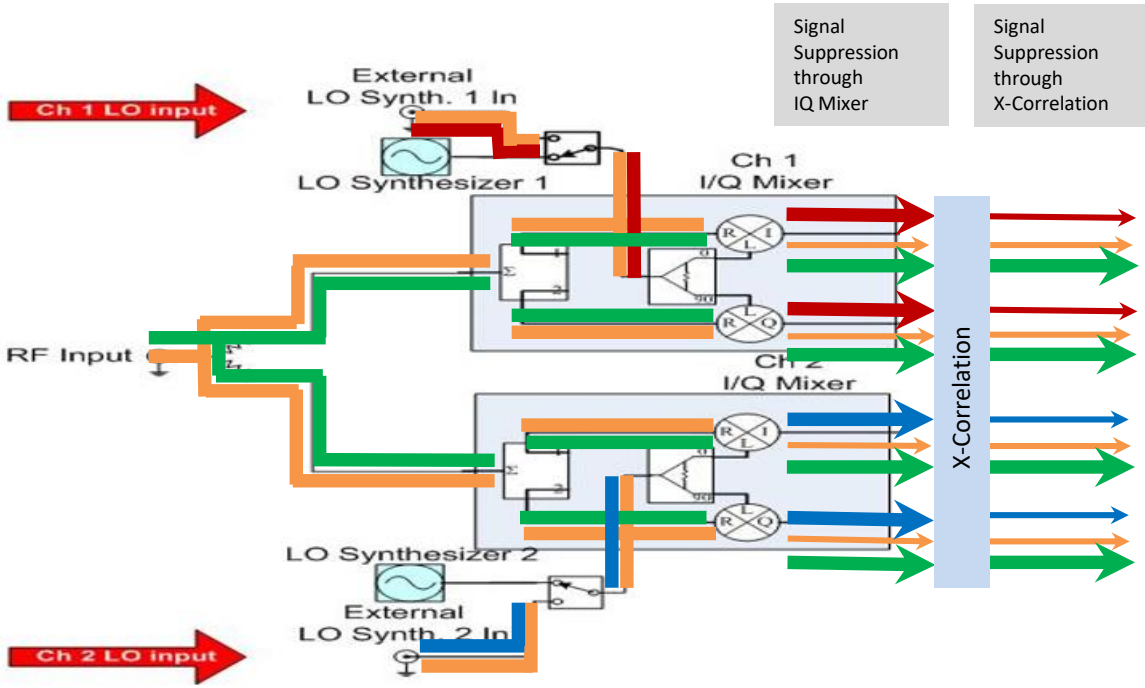


Additive Phase Noise / Jitter

Test of a SerDes PLL (frequency converting)

Example: R&S FSWP



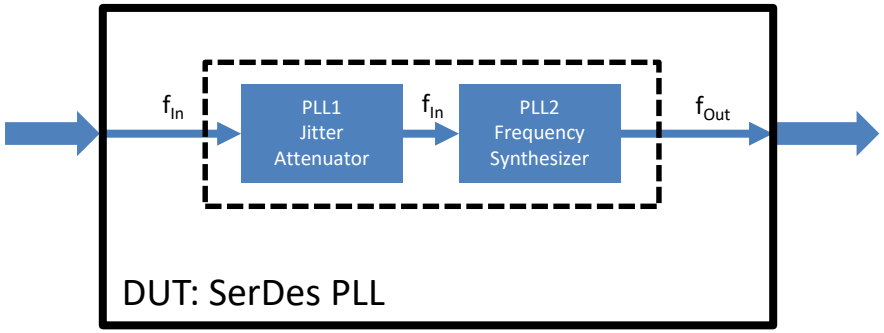


Jitter Attenuation (JTF)

Jitter Transfer Function JTF:

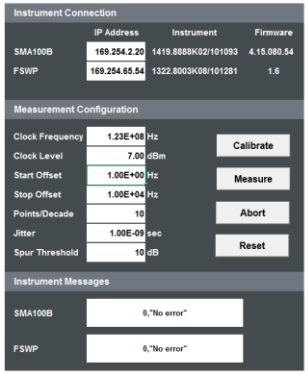
Example: R&S FSWP + R&S SMA100B

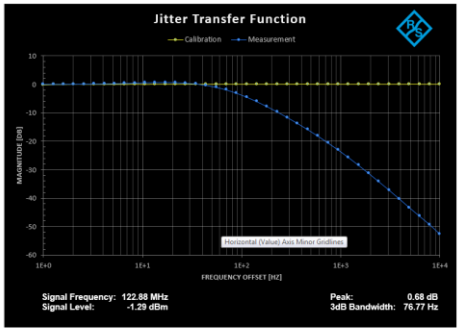
reference clock
$Jitter_{In}$



bit clock
$Jitter_{Out}$

reference clock
with artificial jitter
→ PM modulation





$$JTF = 20 \log \frac{Jitter_{Out}}{Jitter_{In}}$$

Phase Noise Measurement:
1) Calibration w/o DUT
2) Measurement

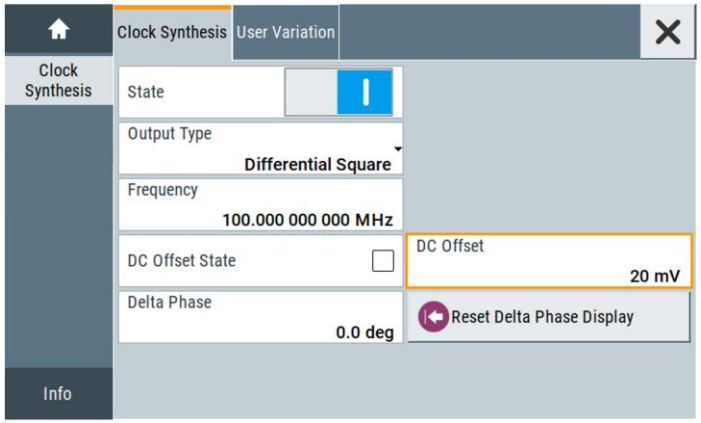
System Margin Test

Example: R&S SMA100B

Refclk

DUT:
SerDes PLL
Reference Design
System Design

reference clock signal:

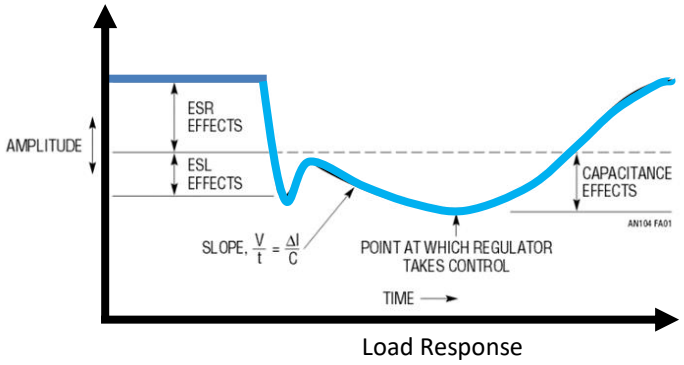


Testing of sensitivity against:
- Slew rate
- DC offset voltage
- …

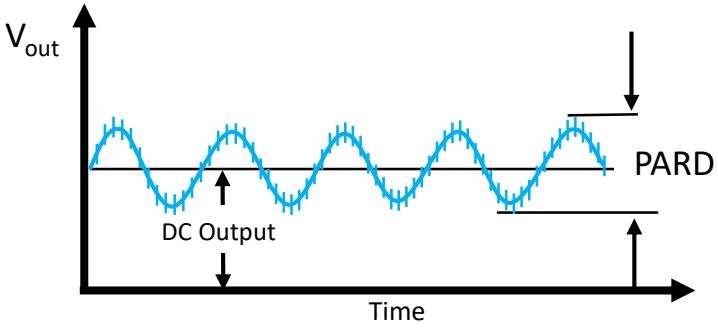
Power Integrity Test

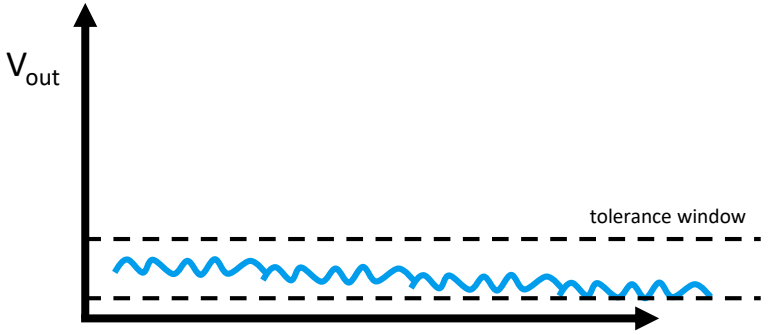
Power Integrity Problems

- PARD (Periodic and Random Disturbances):
  - noise
  - ripple
  - transients
- Static and dynamic load response
- Supply drift



Load Response





Conclusions / Questions

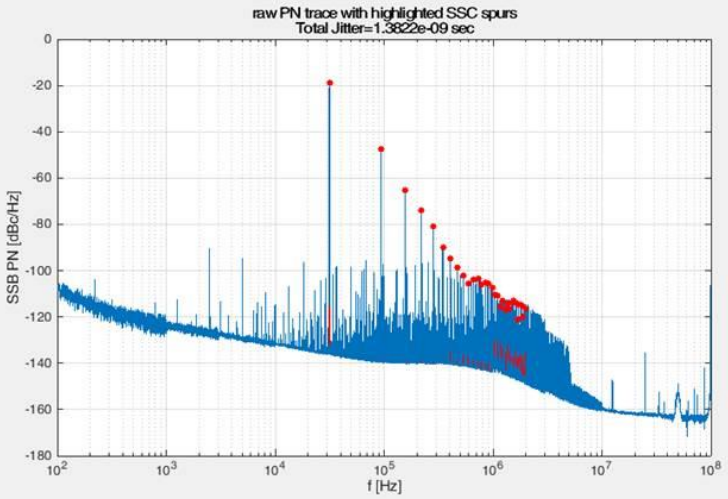
- **For 16.0 GT/s and beyond, PCIe clocks need to meet tighter and tighter jitter limits**
- **Phase Noise Analyzers are the instruments of choice to measure phase noise and jitter on CW and clock signals**
  - **designed for outstanding phase noise / jitter sensitivity**
  - **sensitivity independent of device slew rate**
- **Modern Phase Noise Analyzers provide an accurate, repeatable and user-friendly way to measure low-jitter SSC clocks**
- **Offline Tools are available to convert phase noise into PCIe clock jitter**
- **For further questions and practical demonstrations …**
  - **please visit Rohde & Schwarz at Booth 7**

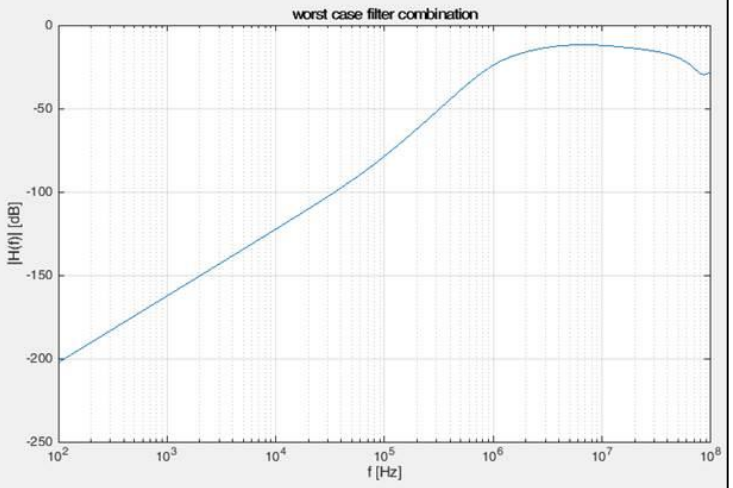
For Further Discussions …

PCIe 4.0 16GT/s
Common Refclk (CC) RMS Jitter

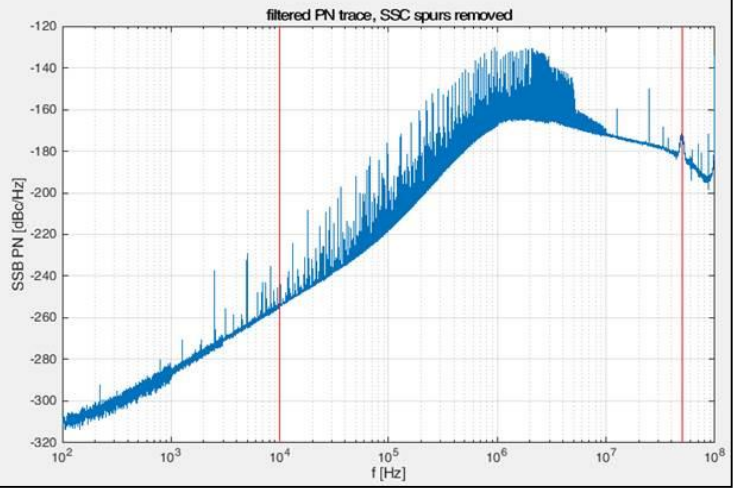
FSWP IP Address	169.254.54.65
Start Offset [Hz]	100
Stop Offset [Hz]	100000000
Integration Range Start [Hz]	10000
Integration Range Stop [Hz]	50000000
RBW [%]	0.1
XCORR Factor	5
Spur Threshold [dB]	6

Measure





	PLL#1 2MHz 0.01dB	PLL#1 2MHz 2dB	PLL#1 4MHz 0.01dB	PLL#1 4MHz 2dB	PLL#2 2MHz 0.01dB	PLL#2 2MHz 1dB	PLL#2 5MHz 0.01dB	PLL#2 5MHz 1dB
PLL#1, 2MHz, 0.01dB	28.26	43.72	77.36	88.60	28.26	23.43	95.07	99.20
PLL#1, 2MHz, 2dB	73.97	23.05	123.75	130.50	73.97	45.35	140.43	**144.88**
PLL#1, 4MHz, 0.01dB	44.72	87.23	42.82	53.86	44.72	65.54	58.26	54.66
PLL#1, 4MHz, 2dB	81.04	100.31	87.54	41.21	81.04	88.45	101.44	82.17
PLL#2, 2MHz, 0.01dB	28.26	43.72	77.36	88.60	28.26	23.43	95.07	99.20
PLL#2, 2MHz, 1dB	50.62	23.01	101.89	110.77	50.62	24.68	119.16	123.83
PLL#2, 5MHz, 0.01dB	58.73	102.99	38.56	55.38	58.73	81.34	49.54	45.07
PLL#2, 5MHz, 1dB	71.98	108.53	56.09	34.69	71.98	90.09	66.82	48.00



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